INTEGRATED CIRCUITS

DATA SHEET

80C51/87C51/80C52/87C52

80C51 8-bit microcontroller family 4 K/8 K OTP/ROM low voltage (2.7 V-5.5 V), low power, high speed (33 MHz), 128/256 B RAM

Product specification Replaces datasheet 80C51/87C51/80C31 of 2000 Jan 20 2000 Aug 07





Philips Semiconductors Product specification

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80C51/87C51/80C52/87C52

DESCRIPTION

The Philips 80C51/87C51/80C52/87C52 is a high-performance static 80C51 design fabricated with Philips high-density CMOS technology with operation from 2.7 V to 5.5 V.

The 8xC51 and 8xC52 contain a 128 \times 8 RAM and 256 \times 8 RAM respectively, 32 I/O lines, three 16-bit counter/timers, a six-source, four-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the device is a low power static design which offers a wide range of operating frequencies down to zero. Two software selectable modes of power reduction—idle mode and power-down mode are available. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative. Since the design is static, the clock can be stopped without loss of user data and then the execution resumed from the point the clock was stopped.

SELECTION TABLE

For applications requiring more ROM and RAM, see the 8XC54/58 and 8XC51RA+/RB+/RC+/80C51RA+ data sheet.

Note: 80C31/80C32 is specified in separate data sheet.

| ROM/EPROM Memory Size (X by 8) | RAM Size (X by 8) | Programmable Timer Counter (PCA) | Hardware Watch Dog Timer | | | | |
|--------------------------------------|----------------------|--|--------------------------------|--|--|--|--|
| 80C31*/80C51/87C51 | | | | | | | |
| 0K/4K | 128 | No | No | | | | |
| 80C32*/80C52/87C52 | | | | | | | |
| 0K/8K/16K/32K | 256 | No | No | | | | |
| 80C51RA+/8XC51RA+/RB+/RC+ | | | | | | | |
| 0K/8K/16K/32K | 512 | Yes | Yes | | | | |
| 8XC51RD+ | | | | | | | |
| 64K | 1024 | Yes | Yes | | | | |

FEATURES

- 8051 Central Processing Unit
 - 4k × 8 ROM (80C51)
 - 8k × 8 ROM (80C52)
 - 128 × 8 RAM (80C51)
 - 256 × 8 RAM (80C52)
 - Three 16-bit counter/timers
 - Boolean processor
- Full static operation
- Low voltage (2.7 V to 5.5 V@ 16 MHz) operation
- Memory addressing capability
- 64k ROM and 64k RAM
- Power control modes:
- Clock can be stopped and resumed
- Idle mode
- Power-down mode
- CMOS and TTL compatible
- TWO speed ranges at V_{CC} = 5 V
 - 0 to 16 MHz
- 0 to 33 MHz
- Three package styles
- Extended temperature ranges
- Dual Data Pointers
- Security bits:
 - ROM (2 bits)
 - OTP/EPROM (3 bits)
- Encryption array 64 bytes
- 4 level priority interrupt
- 6 interrupt sources
- Four 8-bit I/O ports
- Full-duplex enhanced UART
 - Framing error detection
 - Automatic address recognition
- Programmable clock out
- Asynchronous port reset
- Low EMI (inhibit ALE and slew rate controlled outputs)
- Wake-up from Power Down by an external interrupt

80C51 8-bit microcontroller family 4 K/8 K OTP/ROM low voltage (2.7 V-5.5 V), low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

80C51/87C51 ORDERING INFORMATION

| | MEMORY SIZE 4K×8 | TEMPERATURE RANGE °C AND PACKAGE | VOLTAGE RANGE | FREQ. (MHz) | DWG.# |
|-----|---------------------|--|------------------|----------------|----------|
| ROM | P80C51SBPN | O to 170 Pleatic Puel la lies Pechana | 2.7 V to 5.5 V | 0 to 16 | SOT129-1 |
| OTP | P87C51SBPN | 0 to +70, Plastic Dual In-line Package | | | |
| ROM | P80C51SBAA | O to 170 Pleatic Leaded Obio Comics | 2.7 V to 5.5 V | 0 to 16 | SOT187-2 |
| OTP | P87C51SBAA | 0 to +70, Plastic Leaded Chip Carrier | | | |
| ROM | P80C51SBBB | O to 170 Pleatic Oued Flat Peak | 2.7 V to 5.5 V | 0 to 16 | SOT307-2 |
| OTP | P87C51SBBB | 0 to +70, Plastic Quad Flat Pack | | | |
| ROM | P80C51SFPN | 40 to 105 Pleatic Duel la line Package | 2.7 V to 5.5 V | 0 to 16 | SOT129-1 |
| OTP | P87C51SFPN | –40 to +85, Plastic Dual In-line Package | | | |
| ROM | P80C51SFA A | 40 to 405. Pleatic Located Obio Comics | 2.7 V to 5.5 V | 0 to 16 | SOT187-2 |
| OTP | P87C51SFA A | –40 to +85, Plastic Leaded Chip Carrier | | | |
| ROM | P80C51SFBB | 40 to 195 Pleatic Quad Flat Pack | 2.7 V to 5.5 V | 0 to 16 | SOT307-2 |
| OTP | P87C51SFBB | –40 to +85, Plastic Quad Flat Pack | | | |
| ROM | P80C51UBAA | 0 to +70, Plastic Leaded Chip Carrier | 5 V | 0 to 33 | SOT187-2 |
| OTP | P87C51UBAA | 0 to +70, Plastic Leaded Chip Camer | | | |
| ROM | P80C51UBPN | O to 170 Pleatic Duel la line Beek | 5 V | 0 to 33 | SOT129-1 |
| OTP | P87C51UBPN | 0 to +70, Plastic Dual In-line Package | | | |
| ROM | P80C51UFA A | 40 to 195 Plantia Londod Chip Comics | 5 V | 0 to 33 | SOT187-2 |
| OTP | P87C51UFA A | –40 to +85, Plastic Leaded Chip Carrier | | | |

PART NUMBER DERIVATION

| DEVICE NUMBER | DEVICE NUMBER | OPERATING FREQUENCY, MAX (S) | TEMPERATURE RANGE (B) | PACKAGE (AA) |
|------------------|------------------|------------------------------|--------------------------------------|--------------|
| ROM | P80C51 | S = 16 MHz | B = 0° to +70°C | AA = PLCC |
| ROM | P80C52 | S = 16 MHz | B = 0° to +70°C | AA = PLCC |
| OTP | P87C51 | U = 33 MHz | $F = -40^{\circ}C$ to $+85^{\circ}C$ | BB = PQFP |
| OTP | P87C52 | U = 33 MHz | $F = -40^{\circ}C$ to $+85^{\circ}C$ | BB = PQFP |

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